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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/017,737	12/14/2001	Kazuaki Ano	TI-33183	8828

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EXAMINER

LEWIS, MONICA

ART UNIT PAPER NUMBER

2822

DATE MAILED: 10/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/017,737

Applicant(s)

ANO, KAZUAKI

Examiner

Monica Lewis

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-- The MAILING DATE of this communication appears on the cover sheet with the corresponding address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 7/11/03.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5, 7-10, 21, 23-26 and 28-30 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5, 7-10, 21, 23-26 and 28-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 February 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____. 6) ☐ Other: _____

DETAILED ACTION

1. This action is in response to the request for continued examination filed July 11, 2003.

Response to Arguments

2. Applicant's arguments with respect to claims 1-5, 7-10, 21, 23-26, 28-30 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-5 and 7-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear what is meant by the following: a) "thickness cooperable" (See Claim 1); and b) "the super junction structure and is electrically conducted to the second semiconductor region disposed in the peripheral region" (See Claim 1). Claims 2-5 and 7-10 depend directly or indirectly from a rejected claim and are, therefore, also rejected under 35 U.S.C. 112, second paragraph for the reasons set above.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

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6. Claims 1, 3-5, 7, 8, 10, 21, 23-26 and 28-30, as far as understood, are rejected under 35

U.S.C. 102(a) as being anticipated by Derderian (U.S. Publication No. 2003/0038355).

In regards to claim 1, Derderian discloses the following:

a) a first chip (10) having opposing top and bottom surfaces and having bonding pads located on a perimeter of said top surface, each of said bonding pads operable for bonding a wire (For Example: See Figure 9); and

b) a second chip (110) having opposing top and bottom surfaces and having bonding pads located on a perimeter of said top surface, each of said bonding pads operable for bonding a wire (For Example: See Figure 9);

c) a first attach layer having an area equal to an area of said second chip bottom surface for coupling said first chip and said second chip, said first attach layer having a thickness to provide electrical disconnection of said first chip wire bonds and said second chip, said first attach layer is applied to said second chip bottom surface prior to coupling said first chip and said second chip (For Example: See Figure 9); and

d) a second attach layer having an area equal to said second chip bottom surface area and disposed between said first attach layer and said second chip bottom surface, said second attach layer being an insulating material having a thickness cooperable with said first attach layer to provide electrical disconnection of said first chip wire bonds and said second chip (For Example: See Figure 9).

In regards to claim 3, Derderian discloses the following:

a) first attach layer is a thermosetting material, wherein said thermosetting material is pliable for coupling said first chip and said second chip such that said thermosetting material conforms to said first chip wire bond (For Example: See Figure 9 and Paragraphs 62 and 63).

In regards to claim 4, Derderian discloses the following:

a) first chip top and bottom surfaces and said second chip top and bottom surfaces have equal areas (For Example: See Figure 9).

In regards to claim 5, Derderian discloses the following:

a) first chip and said second chip have a stacked arrangement such that said first chip bonding pads are covered from above by said second chip (For Example: See Figure 9).

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In regards to claim 7, Derderian disclose the following:

a) first attach layer is a thermosetting material, wherein said thermosetting material is pliable for coupling said first chip and said second chip such that said thermosetting material conforms to said first chip wire bond and said second attach layer is silicon dioxide (For Example: See Figure 9 and Paragraphs 62 and 63).

In regards to claim 8, Derderian discloses the following:

a) electrical disconnection is provided as a gap between said first chip wire bonds and said second chip, and wherein said gap is approximately equal to said second attach layer thickness (For Example: See Figure 9).

In regards to claim 10, Derderian discloses the following:

a) first chip top and bottom surfaces and said second chip top and bottom surfaces have equal areas, and wherein said first and second chips are stacked such that said first chip bonding pads are covered from above by said second chip (For Example: See Figure 9).

In regards to claim 21, Derderian discloses the following:

a) a first chip having opposing top and bottom surfaces and having first bonding pads located on a perimeter of said top surface (For Example: See Figure 9);

b) a wire having a bond to one of said first bonding pads (For Example: See Figure 9);

c) a second chip having opposing top and bottom surfaces and positioned with said bottom surface adjacent said top surface of said first chip (See Figure 9);

d) a first attach layer between said top surface of said first chip and said bottom surface of said second chip, said first attach area having an area substantially equal to the area of said second chip; and

e) a second attach layer adjacent to said bottom surface of said second chip and between said bottom surface of said second chip and said first attach layer (For Example: See Figure 9)

In regards to claims 23 and 28, Derderian discloses the following:

a) first attach layer is a thermosetting material (For Example: See Paragraphs 62 and 63).

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In regards to claims 24 and 29, Derderian discloses the following:

a) second attach layer is an inorganic material (For Example: See Paragraphs 62 and 63).

In regards to claims 25 and 30, Derderian discloses the following:

a) the first and second chips are approximately the same size (For Example: See Figure 9).

In regards to claim 26, Derderian discloses the following:

a) a first chip having opposing top and bottom surfaces and having first bonding pads located on a perimeter of said top surface, said first chip mounted on said substrate (For Example: See Figure 9);

b) a wire having a ball bond (For Example: See Figure 9);

c) a second chip having opposing top and bottom surfaces and positioned with said bottom surface of said second chip adjacent said top surface of said first chip (For Example: See Figure 9);

d) a first attach layer between said top surface of said first chip and said bottom surface of said second chip and covering said wire bond to said one of said first bonding pads, said first attach layer having an area substantially equal to the area of said second chip (For Example: See Figure 9; and

e) a second attach layer adjacent to said bottom surface of said second chip and between said bottom surface of said second chip and said first attach layer (For Example: See Figure 9).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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8. Claims 2 and 9 are rejected under 35 U.S.C. 103(a) as obvious over Derderian (U.S. Publication No. 2003/0038355).

In regards to claim 2, Derderian fails to disclose the following:

a) electrical disconnection is provided as a gap between said first chip wire bonds and said second chip, and wherein said gap is approximately 10 μm .

However, the applicant has not established the critical nature of the dimension of 10 μm . “The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range.” *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990).

In regards to claim 9, Applicant’s Prior Art fails to disclose the following:

a) second attach layer thickness is approximately 1 μm .

However, the applicant has not established the critical nature of the dimension of 1 μm . “The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range.” *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990).

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Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 703-305-3743.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML

September 24, 2003


AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
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